

# A GaAs HBT 5.8 GHz OFDM Transmitter MMIC Chip Set

A. Raghavan, E. Gebara, C-H. Lee, S. Chakraborty, D. Mukherjee, J. Bhattacharjee, D. Heo and J. Laskar

Yamacraw Design Center, School of Electrical and Computer Engineering, Georgia Institute of Technology, 791 Atlantic Drive, Atlanta, GA 30332-0269, USA. Email: arvindr@ece.gatech.edu

**Abstract** This paper presents a GaAs/AlGaAs HBT transmitter MMIC chip set consisting of a power amplifier, a mixer and a voltage-controlled oscillator (VCO) for 5.8 GHz OFDM applications. The performance of the transmitter in an OFDM system is investigated by means of envelope co-simulation of the circuit in an OFDM transmitter simulation platform that conforms to the IEEE 802.11a wireless LAN standard. To the best of our knowledge, this research represents the first reported implementation of an OFDM transmitter in GaAs HBT technology.

## I. INTRODUCTION

Orthogonal Frequency Division Multiplexing (OFDM), a multi-carrier modulation technique, has been chosen for the IEEE 802.11a standard for high-speed wireless LAN applications in the 5 GHz U-NII bands [1]. While OFDM offers many advantages over conventional single carrier systems such as robustness against multipath fading and narrowband interference [2], the high peak-to-average power (PAP) ratio of the non-constant envelope OFDM signal makes it susceptible to nonlinear distortion from the power amplifier. In order to meet the stringent linearity demands of OFDM, optimized output power back-off is required to reduce signal degradation [3].

GaAs HBTs combine the advantages of a bipolar device with the high frequency performance offered by GaAs technology. Their high linearity, efficiency and breakdown voltage characteristics make them an attractive choice for power amplifier design in the 5 GHz bands. Their exponential output current - input voltage characteristic allows high performance mixing functions to be realized and their low 1/f corner frequency enables the design of low phase noise VCOs [4]. We present a 5.8 GHz GaAs HBT transmitter MMIC chip set for the OFDM system. Initial performance results show a significant improvement over a previous GaAs MESFET implementation [5]. Using a system simulation platform developed in Agilent's Advanced Design System (ADS) according to the IEEE 802.11a standard, we verify the performance of the transmitter.

## II. MMIC DESIGN AND PERFORMANCE

The transmitter chip set comprises a power amplifier, an upconversion mixer and a VCO designed in RF Micro Devices' GaAs/AlGaAs HBT process.

### A. Power Amplifier

The high peak-to-average power ratio of OFDM places a high linearity requirement on the power amplifier (PA). To meet the high linearity specification, there are several solutions such as the use of a feedback, pre-distortion or feedforward mechanism [6]. However, these methods require additional complex circuitry. For compact design, the class A topology, which offers highest linearity, was chosen. The designed PA, shown in Fig. 1, has an area of 1.6 X 1.3 mm<sup>2</sup>.

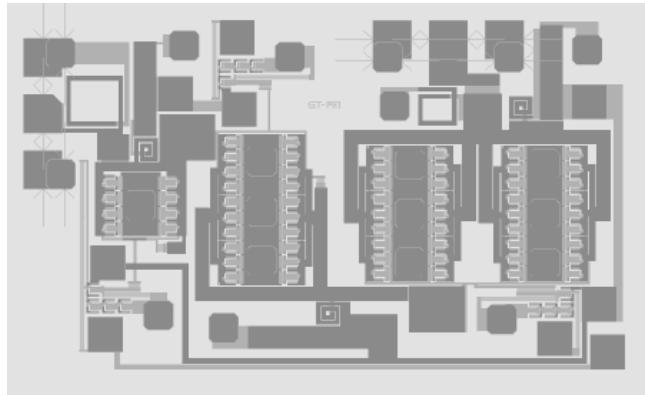


Fig. 1. GaAs HBT OFDM Power Amplifier

The PA consists of three stages with on-chip matching and bias circuits as shown schematically in Fig. 2. The output match network consists of a simple high-pass configuration in order to minimize area. The design of the RF choke is critical since a high inductance is accompanied by a high parasitic resistance resulting in an unacceptable level of loss of dc voltage available at the collectors of the transistors. Hence the RF choke needs to be designed carefully to trade-off the available dc voltage at the collectors of the transistors with the loss of power into the inductor due to its impedance becoming comparable to

that of the output match network. Also, as the inductance of the choke is decreased to reduce its parasitic resistance, it becomes necessary to view the choke itself as part of the matching network. A further consideration is the choice of dc supply voltage to obtain sufficient voltage at the collectors of the devices to achieve the targeted output power. This design uses a dc supply of 5V. RC feedback networks have been provided in the gain stages to enhance stability and emitter degeneration resistances have been included in the power stages to prevent thermal runaway.

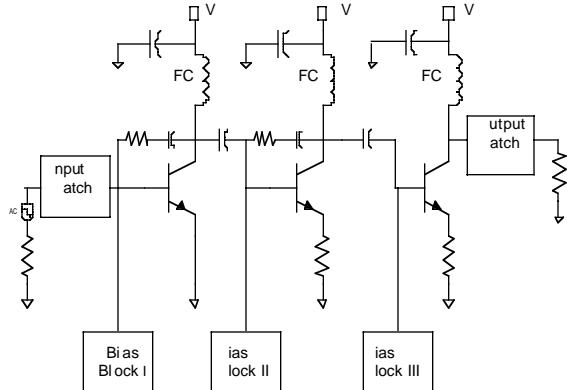


Fig. 2. Schematic of the Power Amplifier

The initial results of performance of the PA are shown in Fig. 3. The PA exhibits an output P1dB of 29 dBm at 5.8 GHz with a power gain of 20 dB at P1dB. The output IP3 is 33 dBm at P1dB at 5.8 GHz. The IMD3 at 3.5 dB back-off is approximately 30 dBc. These results compare favorably with a previous GaAs MESFET implementation [5] while significantly reducing the chip area. Another implementation of the PA with the output match and RF chokes off-chip has been designed to take advantage of the improved performance of off-chip passive components.

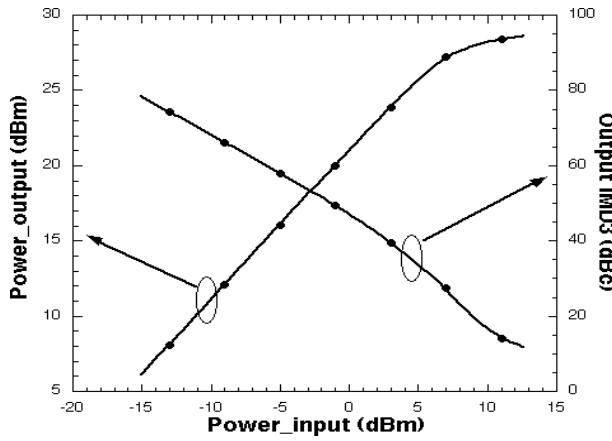


Fig. 3. Initial performance of the PA at 5.8 GHz

### B. Mixer

The upconversion mixer uses a double balanced Gilbert cell topology. It occupies an area of  $2 \times 1 \text{ mm}^2$  as shown in Fig. 4. It has a buffer on the LO side which facilitates a low input LO drive (-5 dBm) while maintaining a high input power to the switching quad which is needed to reduce the noise figure of the mixer. It also tolerates a relatively large input LO power fluctuation without significantly affecting the performance of the switching quad. The input (RF) match is on-chip and the output (IF) match is off-chip, which enables the circuit to be used for up as well as down conversion. Both the LO buffer and the emitter follower are current-controlled to optimize gain and noise performance. Differential probes and a coupler are needed to measure the mixer performance due to its double balanced topology.

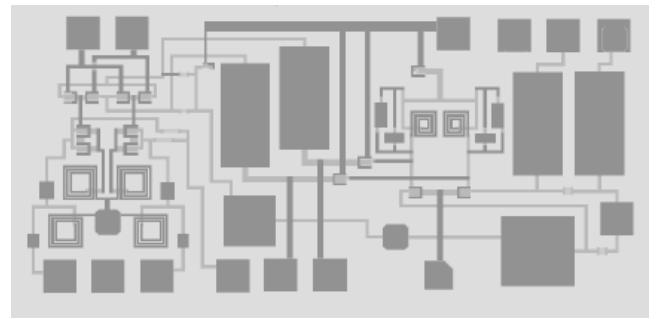


Fig. 4. GaAs HBT Gilbert cell upconversion mixer

The mixer is designed for an input IF range of 0.9 - 1.1 GHz with an output RF range of 5.7 - 5.9 GHz. It has a conversion gain of 2 dB, an IIP3 of 5 dBm and a NF of 15 dB. It operates at a dc supply of 5V. These results are a significant improvement over the performance reported previously in [5].

### C. Voltage Controlled Oscillator

The common-base (CB) negative resistance topology with series inductive feedback is used for VCO design. A series inductance in the base provides the necessary negative output resistance. The Schottky barrier diode is used to tune the impedance of the input port of the series-feedback oscillator by varying the varactor capacitance. The circuit occupies an area of  $0.68 \times 0.67 \text{ mm}^2$  as shown in Fig. 5. The monolithic VCO employs a HBT with 4 emitter fingers ( $2 \mu\text{m} \times 20 \mu\text{m}$  each) for negative resistance generation and a Schottky diode ( $15 \mu\text{m} \times 15 \mu\text{m}$ ) in the resonator to provide frequency tuning. Bias networks for the HBT and Schottky diode are implemented on-chip.

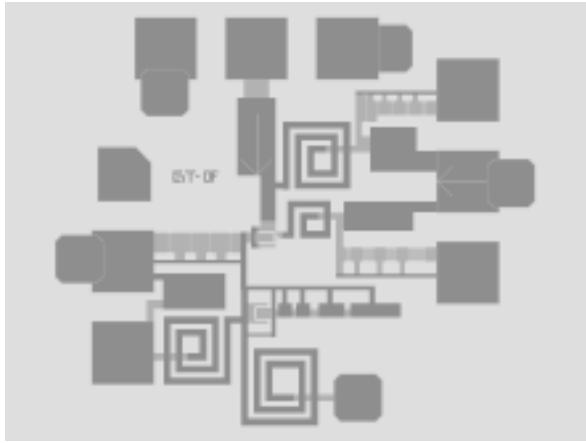


Fig. 5. OFDM GaAs HBT VCO

The VCO has a frequency tuning range of 400MHz from 4.65 to 6.05 GHz with an output power of  $9 \pm 0.5$  dBm over a tuning voltage range of 0.25 to 1.25 V as shown in Fig. 6. All the harmonics and spurs are less than  $-25$  dBc. These characteristics have been achieved without any buffer amplifiers.

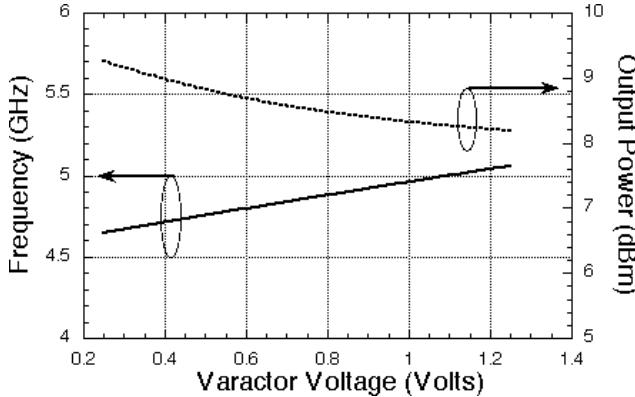


Fig. 6. Frequency tuning performance of the VCO

### III. SYSTEM PERFORMANCE

To test the performance of the designed transmitter in an OFDM system, a system simulation platform has been developed in accordance with the IEEE 802.11a standard [1]. The schematic representation of the OFDM transmitter model is shown in Fig. 7. Simulation parameters have been set in compliance with IEEE 802.11a. Data throughput (uncoded) is taken to be 24 Mbits/s. The data bits are scrambled and encoded using a rate 1/2 convolution code with constraint length 7. The coded sequence is mapped into a 16-QAM constellation. Then virtual carriers

are inserted and the QAM symbols are transformed from frequency domain to time domain using 64 point IFFT. After inserting cyclic prefix, the IFFT output is I/Q modulated to an IF frequency of 1 GHz. Raised cosine filtering is performed for symbol shaping. Filtered OFDM symbols are upconverted to 5.8 GHz and fed to the power amplifier.

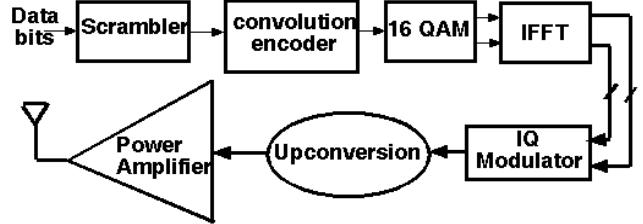


Fig. 7. Block diagram of the simulation model

The system simulation model is implemented in Agilent's ADS (Advanced Design System). Since the power amplifier is the most critical component of the RF portion of the system, circuit envelope co-simulation of the PA is incorporated in the system simulation set-up for better accuracy while ADS behavioral models are used for the mixer and the VCO to reduce simulation time and effort. The output spectra resulting from the simulations are shown in Fig. 8.

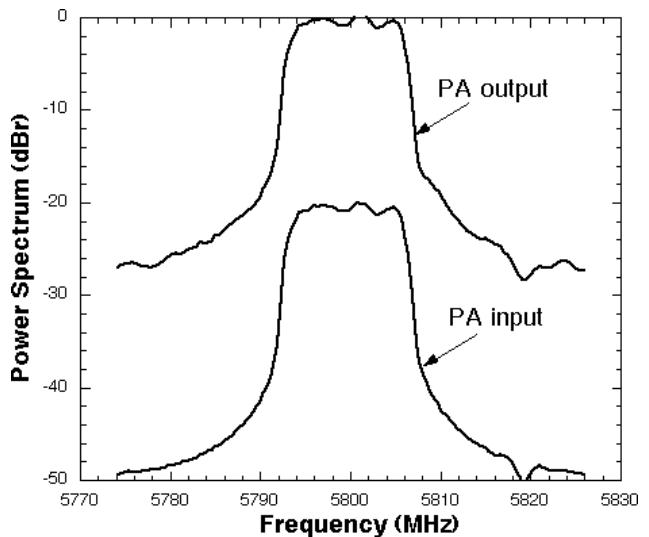


Fig. 8. Power spectra from system simulation

It is seen from the figure that the non-linearities of the PA have resulted in a spectral regrowth at its output. In the simulation, the output power has been backed off sufficiently (12 dB) to meet the spectrum mask requirements of the standard [1]. This is significantly lesser

than the 18 dB back-off predicted by merely considering the number of carriers (64), the reason being that as the number of carriers becomes large, the OFDM signal distribution tends to the Gaussian distribution [3].

#### IV. CONCLUSION

A GaAs HBT OFDM transmitter chip set has been designed and its performance in an OFDM transmitter system studied. The upconversion Gilbert cell mixer shows a good conversion gain and good linearity. The VCO has been designed for good noise performance. The GaAs HBT power amplifier has been designed to meet the high linearity demands of OFDM as well as with a view to achieving a compact implementation. Circuit envelope simulation of the power amplifier in an OFDM system indicate a back-off requirement of 12 dB to fit the output spectrum mask of IEEE 802.11a. This back-off requirement can be reduced by increasing the number of carriers since the OFDM signal then tends to the Gaussian distribution which has a PAP of 9 dB [7]. Also, the peak-to-average power (PAP) ratio of the OFDM signal itself can be reduced substantially using techniques such as clipping, peak windowing and peak cancellation or by using PAP reduction codes [2].

#### ACKNOWLEDGEMENT

The authors wish to acknowledge the support of RF Micro Devices with special thanks to Bruce Schumkler and Chris Arnott and the Yamacraw Design Center.

#### REFERENCES

- [1] IEEE Draft Supplement to IEEE Std. 802.11, Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) specifications: High-speed physical layer in the 5 GHz band, September 1999.
- [2] Richard Van Nee and Ramjee Prasad, *OFDM for Wireless Multimedia Communications*, Artech House Publishers, 2000.
- [3] S. Merchan, A. Garcia Armada and J. L. Garcia, "OFDM performance in amplifier nonlinearity," *IEEE Trans. Broadcasting*, vol. 44, no. 1, pp. 106-114, March 1996.
- [4] M. E. Kim, A. K. Oki, G. M. Gorman, D. K. Umemoto and J. B. Camou, "GaAs heterojunction bipolar transistor device and IC technology for high-performance analog and microwave applications," *IEEE Trans. Microwave Theory and Tech.*, vol. 37, no. 9, pp. 1286-1303, September 1989.
- [5] S. Yoo, D. Heo, C-H. Lee, B. Matinpour, S. Chakraborty and J. Laskar, "A 5.8 GHz OFDM GaAs MESFET MMIC chip set," *2000 IEEE MTT-S Int. Microwave Symp. Dig.*, vol. 3, pp. 1273-1276, June 2000.
- [6] M. Hayashi, M. Nakatsugawa and M. Muraguchi, "Quasi-linear amplification using self phase distortion compensation technique," *IEEE Trans. Microwave Theory and Tech.*, vol. 43, no.11, pp. 2557-2564, November 1995.
- [7] Steve C. Cripps, *RF Power Amplifiers for Wireless Communications*, Artech House Publishers, 1999.